REMARKS

This responds to the Office Action mailed on September 27, 2004.

Claims 4, 6, and 10 are amended, no claims are canceled or added; as a result, claims 1–15 are now pending in this application.

Objections as to some claims

Claims 4 and 10 were objected to because of the following informalities:

In claim 4, line 13 a period (".") at the end of the line is missing.

In claim 10, line 13, a "0" should be deleted.

Appropriate correction has been made.

Allowable Subject Matter

Claims 6-7 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 has been rewritten in independent form including all of the limitations of claim 1, the base claim and intervening dependant claims 2 and 3. Claim 7 which is dependant upon claim 6 is also allowable in view of the amendment to claim 6.

Claims 4-5 and 10-12 were indicated to be allowable if rewritten to overcome the minor informalities set forth in the Office Action.

Claims 4 and 10 were amended to correct the informalities pointed out in the Office Action. Those amendments did not change the scope of those claims. They and their dependant claims 5, 11 and 12 are all believed to be allowable.

In view of the amendments discussed above, reconsideration and allowance of claims 4–7 and 10–12 is respectfully requested.

§103 Rejection of the Claims

Claims 1-3, 8, 9, and 13-15 were rejected under 35 USC § 103(a) as being unpatentable over Jeddeloh (U.S. 6,401,213) in view of Churchill et al. (U.S. 6,286,118).

The cited Jeddeloh patent relates to a timing circuit using a delay circuit to adjustably delay and generate a data strobe signal. It determines a timing relationship between a sampled clock signal and a sampled data signal to allow optimal delay of a read data strobe to transition in the middle of a data signal's data eye. It does not determine timing margins.

The cited Churchill patent relates to "test mode features for integrated circuits."[1] More specifically it relates to "adjusting or varying the timing of the clock signal input into sense amplifier(s) 214 (SACLK) enables one to characterize timing margins or to determine if timing of the SACLK signal is causing observed errors at the output of output register 210.[2]

Independent claims1, 8 and 13, by way of example, each call for a system for determining time margins between data and strobe signals. The claimed invention does not determine time margins between a clock signal and a sampled data signal as Jeddeloh apparently does; rather it measures the margin between data and strobe signals. Churchill was cited for what was contended to be its "teaching of varying the delay to determine the timing margins..."[3] but does not show measuring time margin between data and strobe signals, as claimed.]The Office Action does not point to anything in Churchill or Jeddeloh that can be combined to provide a system measuring time margin between data and strobe signals as claimed in any of claims 1, 8 and 13.

In order to set forth a *prima facie* case of obviousness by combining two patents, an Office Action is required to provide evidence of a motivation or a suggestion to combine the patents as proposed and evidence of a reasonable expectation of success if the combination is made.[4] Additionally, the proposed combination must include all of the elements of the claim.[5] Here there was no evidence of a suggestion or motivation to combine Jeddeloh and Churchill in the manner proposed in the Office Action. It is insufficient to suggest that such evidence is provided merely by alleging "they both teach method for varying the delay of a signal"[6] Furthermore, even if combined, they do not deal with the margin between the same signals required in each of claims 1, 8 and 13. The Office Action does not provide evidence that

[1] Churchill 6,286,118; Col 1, lines 22–23.
[2] Churchill Col 7, lines 46–51.
[3] Office Action page 4, lines 4-5.
[4] MPEP 2143 OA page 4, lines 6-7
[5] MPEP 2143.03
[6] Office Action page 4 lines 2–3.

Jeddeloh and Churchill, taken singly or in combination, teach or suggest structure to determine timing margin between data and strobe signals as independent claims 1 and 8 require. Reconsideration and allowance of claims 1, 8 and 13 and each of their dependent claims is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney ((612) 373-6970) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

GIRISH P. RAMANATHAN ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
(612) 373-6970

Date November 29, 2004 By _____
Charles E. Steffey
Reg. No. 25,179

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29th day of November, 2004.

Amy Moriarty _____
Name Signature